AMENDMENTS TO THE CLAIMS

1. (Previously Presented) An apparatus comprising:

an observability buffer having a trigger, wherein the observability buffer is integrated on a first component which is capable of being communicably coupled with a second component via a simultaneous bi-directional (SBD) interface having ternary logic levels, wherein the observability buffer is configured to un-intrusively observe and echo one or more of a plurality of signals transmitted between the first component and the second component based on one or more of a control signal-based indication, an address signal-based indication, and a time-based indication; and

an observability port on the first component capable of receiving the echoed signals from the observability buffer and providing a diagnostic device access to the echoed signals.

2-5. (Cancelled)

6. (Previously Presented) A method comprising:

transmitting a plurality of signals between a first component and a second component on a simultaneous bi-directional (SBD) interface having ternary logic levels, wherein the first component includes an observability buffer integrated on the first component;

un-intrusively observing one or more of the plurality of signals transmitted on the SBD interface; and

echoing the one or more of the plurality of observed signals to an observability port integrated on the first device based on a received trigger signal, wherein the observability port is capable of interfacing with a diagnostic

device, relaying the echoed signals to the diagnostic device, and includes a logic observability port.

7-13. (Cancelled)

14. (Currently Amended) A system comprising:

a memory communicably coupled with a microprocessor, wherein the microprocessor includes an integrated observability buffer;

a first component communicably coupled to the microprocessor through a simultaneous bi-directional (SBD) interface having ternary logic levels;

wherein the observability buffer coupled with a second component further coupled with a simultaneous bi-directional (SBD) memory bus having ternary logic levels, the trigger to facilitate one or more of un-intrusively observing, reading, and echoing observes and echoes at least one of a plurality of signals transmitted on the SBD memory bus, interface between the first component and the microprocessor; wherein the trigger to instruct the buffer via one or more of a control signal-based indication, an address signal-based indication, and a time-based indication;

an observability port communicably coupled with the observability buffer, the observability port to receive the echoed signals, wherein the observability port includes a logic observability port; and

a diagnostic device communicably coupled with the observability buffer by interfacing with the observability port, wherein the diagnostic device is capable of one or more of detecting, accessing, and reading of the echoed signals.

15-22 (Cancelled)

23. (Previously Presented) The system of claim 14, wherein the diagnostic device comprises one or more of a logic analyzer and a bus analyzer, the diagnostic device coupled to an observability bus, the observability bus further coupled to the observability port.

24. (Previously Presented) The system of claim 14, wherein the plurality of signals are communicated via a wireless communication.

25. (Previously Presented) The system of claim 14, wherein the plurality of echoed signals comprise frequencies between a minimum frequency of 5 gigahertz (GHz) and a maximum frequency of 500 gigahertz (GHz).

26. (Previously Presented) The apparatus of claim 1, wherein the diagnostic device comprises one or more of a logic analyzer and a bus analyzer, the diagnostic device coupled to an observability bus, the observability bus further coupled to the observability port.

27. (Previously Presented) The apparatus of claim 1, wherein the plurality of signals are communicated via a wireless communication.

28. (Previously Presented) The apparatus of claim 1, wherein the echoed signals comprise frequencies between a minimum frequency of 5 gigahertz (GHz) and a maximum frequency of 500 gigahertz (GHz).

29. (Previously Presented) The method of claim 6, wherein the diagnostic device comprises one or more of a logic analyzer and a bus analyzer, the diagnostic device coupled to an observability bus, the observability bus further coupled to the observability port.

30. (Previously Presented) The method of claim 6, further comprising

communicating the plurality of signals via a wireless communication.

31. (Previously Presented) The method of claim 6, wherein the echoed signals comprise frequencies between a minimum frequency of 5 gigahertz (GHz) and a maximum frequency of 500 gigahertz (GHz).

32–35 (Cancelled)